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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/605,193	09/14/2003	William Mar	VIAP0063USA	2192

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NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
P.O. BOX 506
MERRIFIELD, VA 22116

EXAMINER
TRAN, VINCENT HUY

ART UNIT	PAPER NUMBER
2115	

DATE MAILED: 11/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/605,193	MAR ET AL.	
	Examiner	Art Unit	
	Vincent T. Tran	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,8-13 and 15-20* is/are rejected.

7)☒ Claim(s) *6,7 and 14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-20 are pending for examination.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-5, 8-13, 15-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Admitted Prior Art (AP) in view of Wolaver U.S. 4,590,602.

4. As per claim 1, AP teach a method for locking phase by providing a clock synchronized with an input signal, the input signal comprising a plurality of data, the method comprising:

generating an estimated rate according to transitions of the input signal;

adjusting a frequency of the clock synchronized with an input signal according to the updated estimated rate the frequency of the clock correspond to the estimated rate. However, AP do not teach the processing a dithering step for updating the estimated rate by multiplying the estimated rate by a predetermined ratio and modifying the predetermined ratio so that another dithering step may apply the modified predetermined ratio to update the estimated rate.

Wolaver teaches another method of locking phase for digital data communications having data input means, phase lock loop, clock recovery means, and wide rang frequency synthesizer means. Specifically, Wolaver teaches the generating an estimate rate according to the input signal [col. 4 lines 31-30];

processing a dithering step for updating the estimated rate by multiplying the estimated rate by a predetermined ratio [col. 5 lines 35-44; fig. 2];

adjusting a frequency of the clock synchronized with an input signal according to the update estimated rate in the dithering step to make the frequency of the clock correspond to the updated estimated rate [col. 46-54]; and

modifying the predetermined ratio so that another dithering step may apply the modified predetermined ratio to updated the estimate rate [col. 5 lines 64-68; col. 7 lines 35].

AP and Wolaver are analogous art because they from the same field of endeavor – clock synchronized.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to have modified the system of AP with the dithering step of Wolaver to updating the estimated rate to make the frequency of the clock correspond to the update estimated rate.

The motivation for doing so would have been to provide the system with the ability to lock onto the clock or data rate at a higher frequencies range and at a shorter acquisition time [col. 2 lines 49-51].

Therefore, it would have been obvious to combine AP with Wolaver to obtain the invention as specified in claim 1.

5. As per claim 2, Wolaver teaches the predetermined ratio will not vary with the change of the estimated rate in the dithering step when processing the dithering step [fig. 2].

6. As per claim 3, Wolaver teaches changing the predetermined ratios of the adjacent dithering steps according to a predetermine rule [col. 6 lines 3-19].

7. As per claim 4, Admitted Prior Art.

8. As per claim 5, Wolaver teaches before adjusting the frequency of the clock according to the updated estimated rate in the dithering step, a judgment step is processed according to a phase difference of frequency difference [20, 80 fig. 1] between the clock and the input signal to decide whether the frequency of the clock is adjusted according to the updated estimated rate in the dithering step [abs and col. 5 lines 35-44].

9. As per claim 8, AP teach phase lock circuit for providing a clock synchronized with an input signal, the input signal comprising a plurality of data, the phase lock circuit comprising:

a measuring module for generating an estimated rate according to transitions of the input signal;

an oscillator for adjusting a frequency of the clock synchronized with an input signal according to the estimated rate. However, AP does not teach a dithering module coupled to the measuring module for updating the estimated rate by multiplying the estimated rate by a predetermined ratio.

Wolaver teaches another method of locking phase for digital data communications having data input means, phase lock loop, clock recovery means, and wide rang frequency synthesizer means. Specifically, Wolaver teaches a dithering module [50 fig. 1] coupled to the measuring module [20, 80, 40 fig. 1] for updating the estimated rate by multiplying the estimated rate by a predetermined ratio [col. 5 lines 35-44]; and

an oscillator [60 fig. 1] for adjusting a frequency of the lock synchronized with an input signal according to the update estimated rate in the dithering module to make the frequency of the clock correspond to the update estimated rate; wherein after the dithering module updates the estimated rate, the predetermined ratio is modified to multiply the estimated rate by a modified predetermined ratio for updating the estimated rate in the dithering module when the dithering module generates another updated estimated rate [col. 3 lines 46-54].

AP and Wolaver are analogous art because they from the same field of endeavor – clock synchronized.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to have modified the system of AP with the dithering step of Wolaver to updating the estimated rate to make the frequency of the clock correspond to the update estimated rate.

The motivation for doing so would have been to provide the system with the ability to lock onto the clock or data rate at a higher frequencies range and at a shorter acquisition time [col. 2 lines 49-51].

Therefore, it would have been obvious to combine AP with Wolaver to obtain the invention as specified in claim 8.

10. As per claim 9, see claim 2.

11. As per claim 10, see claim 3.

12. As per claim 11, Admitted Prior Art.

13. As per claim 12, AP teach a detecting circuit for deciding whether the estimated rate of the dithering module is transmitted to the oscillator to adjust the frequency of the clock according to the phase difference of frequency difference between the clock and the input signal. However, AP does not teach the estimated rate is updated. Wolaver teaches the updated of the estimated rate [see discussion in claim 1].

14. As per claim 13, AP teach if the detecting circuit detects that the phase difference or the frequency difference between the clock and the input signal exceeds a predetermined value, the estimated rate of the measuring module is transmitted to the oscillator. However, AP does the dithering module to update the estimated rate. Wolaver teaches a dithering module to update the estimated rate [see discussion in claim 1].

15. As per claim 15, AP teach a method for locking phase by providing a comparing clock synchronized with an input signal, the input signal comprising a plurality of data, the method comprising:

generating a frequency adjustment value according to the input signal;

generating a estimated value according to the input signal;

setting a estimated value as a new comparing clock when a synchronization error between the comparing clock and the input signal exceeds a predetermined value; and

comparing the new comparing clock with the input signal in order to adjust the new comparing clock. However, AP does not teach generating a dithering estimate value [a dithering module to update the estimated value] through a dithering step.

Wolaver teaches another method for generating a frequency value according to the input signal. Specifically, Wolaver teaches generating a dithering estimate value according to the input signal through a dithering step and setting a dithering estimated value a new comparing clock [col. 5 lines 35-44].

AP and Wolaver are analogous art because they from the same field of endeavor – clock synchronized.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to have modified the system of AP with the generating of a estimated value through a dithering step of Wolaver to updating the estimated rate to make the frequency of the clock correspond to the update estimated rate.

The motivation for doing so would have been to provide the system with the ability to lock onto the clock or data rate at a higher frequencies range and at a shorter acquisition time [col. 2 lines 49-51].

Therefore, it would have been obvious to combine AP with Wolaver to obtain the invention as specified in claim 8.

16. As per claim 16, see discussion in claim 1.

17. As per claim 17, see discussion in claim 2.

18. As per claim 18, see discussion in claim 3.

19. As per claim 19, Admitted Prior Art.

20. As per claim 20, AP teaches generating an estimated rate according to the number of sampling cycles in a predetermined period of time and the number of the changes of signal level of the input signal in the predetermined period; and

Wolaver teaches generating the dithering estimated value in the dithering step according to the estimated rate [see discussion in claim 1].

Allowable Subject Matter

21. Claim 6,7 and 14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vincent T. Tran whose telephone number is (571) 272-7210. The examiner can normally be reached on 7:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas c. Lee can be reached on (57 1)272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vincent Tran